CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A circuit configuration in switched op-amp technology, comprising:

at least one switchable operational amplifier having an input and an output and transistors having a switching speed;

at least one sampling capacitor connected to said input;

at least one integrating capacitor connected to said input and to said output;

a detector for detecting the switching speed of said transistors, said detector being connected to said operational amplifier;

a clock generator producing a first and a second switching signal each having switching-clock phases including an on-phase and an off-phase, the on-phases of said first and said second switching clock signal being non-overlapping;

said clock generator controlling charging of said sampling capacitor with said first switching-clock signal and switching said operational amplifier on and off with said second switching-clock signal; and

a phase-variance device varying said switching-clock phases in which said first and second switching-clock signals are in said off-phase, said phase-variance device connected to said clock generator, said phase-variance device being configured for varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low.

Claim 2 (original). The circuit configuration according to claim 1, wherein said phase-variance device is configured to vary each of said switching-clock phases in which said first and second switching-clock signals are in said off-phase.

Claim 3 (original). The circuit configuration according to claim 1, wherein said phase-variance device is configured to vary each second one of said switching-clock phases in which

said first and second switching-clock signals are in said off-phase.

Claim 4 (original). The circuit configuration according to claim 1, wherein:

said operational amplifier has a transient response; and

said phase-variance device is configured to vary a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said transient response of said operational amplifier.

Claim 5 (original). The circuit configuration according to claim 1, wherein:

said operational amplifier has transistors having a switching speed; and

said phase-variance device is configured to vary a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors.

Claim 6 (canceled).

Claim 7 (previously presented). The circuit configuration according to claim 1, wherein:

said transistors include at least one of:

n-channel FETs; and

p-channel FETs;

said transistors each have a respective switching speed; and

said detector separately detects said switching speed of said n-channel FETs and said p-channel FETs.

Claim 8 (previously presented). The circuit configuration according to claim 1, including an inverter chain, said detector having one of:

an XOR gate with XOR inputs, one of said XOR inputs receiving an undelayed edge signal, and another of said XOR inputs receiving the edge signal delayed through said inverter chain; and

an XNOR gate with XNOR inputs, one of said XNOR inputs receiving the edge signal and another of said XNOR inputs receiving the edge signal delayed through said inverter chain.

Claim 9 (previously presented). The circuit configuration according to claim 1, wherein said detector generates detector pulses having a duration characterizing said switching speed of said transistors.

Claim 10 (original). The circuit configuration according to claim 9, wherein said phase-variance device is configured to adjust a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon a duration of said detector pulses.

Claim 11 (original). The circuit configuration according to claim 1, wherein said phase-variance device is configured to adjust a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase in a given number of predetermined steps.

Claim 12 (original). The circuit configuration according to claim 1, wherein said clock generator and said phase-variance device are embodied as a programmable clock generator.

Claim 13 (original). The circuit configuration according to claim 1, wherein said clock generator and said phase-variance device are embodied as:

an external squarewave generator producing a squarewave signal; and

a divider circuit connected to said squarewave generator, said divider circuit generating said at least two switching-clock signals from said squarewave signal.

Claim 14 (original). The circuit configuration according to claim 13, wherein:

said squarewave signal has a duty ratio; and

adjustment of said duty ratio varies said switching-clock phases in which said first and second switching-clock signals are in said off-phase.

Claim 15 (currently amended). A circuit configuration in fully differential circuit technology, comprising:

at least one switchable operational amplifier having an input and an output and transistors having a switching speed;

at least one sampling capacitor connected to said input;

at least one integrating capacitor connected to said input and to said output;

a detector for detecting the switching speed of said transistors, said detector being connected to said operational amplifier;

a clock generator producing a first and a second switching signal each having switching-clock phases including an on-phase and an off-phase, the on-phases of said first and said second switching clock signal being non-overlapping;

said clock generator controlling charging of said sampling capacitor with said first switching-clock signal and switching said operational amplifier on and off with said second switching-clock signal; and

a phase-variance device varying said switching-clock phases in which said first and second switching-clock signals are in said off-phase, said phase-variance device connected to said clock generator, said phase-variance device being configured for varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-

phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low.

Claim 16 (currently amended) A circuit configuration in switched op-amp technology, comprising:

at least one switchable operational amplifier having an input and an output and transistors having a switching speed;

at least one sampling capacitor connected to said input;

at least one integrating capacitor connected to said input and to said output;

a detector for detecting the switching speed of said transistors, said detector being connected to said operational amplifier;

clock generator means for generating a first and a second switching signal each having an on-phase and an off-phase, the on-phases of said first and said second switching clock signal being non-overlapping;

said clock generator means controlling charging of said sampling capacitor with said first switching-clock signal and switching said operational amplifier on and off with said second switching-clock signal; and

phase-variance means for varying switching-clock phases in which said first and second switching-clock signals are in said off-phase, said phase-variance means connected to said clock generator means, said phase-variance means being configured for varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low.

Claim 17 (currently amended). A method for clocking successive operational amplifier stages constructed in switched op-amp technology, which comprises:

generating at least two non-overlapping switching-clock signals;

switching a first operational amplifier on and off with a first signal of the two switching-clock signals;

switching a second operational amplifier on and off with a second signal of the switching-clock signals; ~~and~~

varying switching-clock phases of the first and second signals in which the operational amplifiers are switched off; and

providing a variable delay between the switching-clock phases of the first and second signals during which the operational amplifiers are switched off.

Claim 18 (original). The method according to claim 17, which further comprises varying each of the switching-clock phases in which the operational amplifiers are switched off.

Claim 19 (original). The method according to claim 17, which further comprises varying each second one of the switching-clock phases in which the operational amplifiers are switched off.

Claim 20 (original). The method according to claim 17, which further comprises varying a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a transient response of the operational amplifiers.

Claim 21 (original). The method according to claim 17, which further comprises varying a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a switching speed of transistors of the operational amplifiers.

Claim 22 (original). The method according to claim 17, which further comprises separately detecting at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs.

Claim 23 (original). The method according to claim 21, which further comprises separately detecting at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs.

Claim 24 (original). The method according to claim 17, which further comprises adjusting a duration of the switching-clock phases in which the operational amplifiers are switched off in a number of predetermined steps.

Claim 25 (original). The method according to claim 17, which further comprises generating the at least two non-overlapping switching-clock signals with a programmable clock generator.

Claim 26 (original). The method according to claim 17, which further comprises generating the at least two non-overlapping

switching-clock signals with an external squarewave generator and a divider circuit.

Claim 27 (original). The method according to claim 26, which further comprises varying the switching-clock phases in which the operational amplifiers are switched off by adjusting a duty ratio of a squarewave signal from the squarewave generator.

Claim 28 (new). The method according to claim 17, which further comprises varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low.

Claim 29 (new). The method according to claim 17, which further comprises:

providing said transistors with at least one of:

n-channel FETs; and

p-channel FETs;

said transistors each having a respective switching speed; and

separately detecting said switching speed of said n-channel FETs and said p-channel FETs.

Claim 30 (new). The circuit configuration according to claim 15, wherein:

said transistors include at least one of:

n-channel FETs; and

p-channel FETs;

said transistors each have a respective switching speed; and

said detector separately detects said switching speed of said n-channel FETs and said p-channel FETs.

Claim 31 (new). The circuit configuration according to claim 16, wherein:

said transistors include at least one of:

n-channel FETs; and

p-channel FETs;

said transistors each have a respective switching speed; and

said detector separately detects said switching speed of said n-channel FETs and said p-channel FETs.